IN THE CLAIMS

Please add new claims 31 and 32.

Please amend claims 1-3, 7, 8, 14, 17, 19-22, 28, and 30 as follows:

1. (Currently Amended) A magnetic memory, comprising:

an array of memory cells configured to provide first logic value and second logic value resistive states; and

a read circuit configured to sense a resistance through a memory cell in the array of memory cells to obtain a sense result and categorize the sense result into one of at least three different categories comprising a middle category situated between the first logic value and second logic value resistive states.

2. (Currently Amended) The magnetic memory of claim 1, where the at least three different categories comprise a first logic value ~~low~~ resistive state category and a second logic value~~high~~ resistive state category, where the middle category is situated between the first logic value~~low~~ resistive state category and the second logic value~~high~~ resistive state category.

3. (Currently Amended) The magnetic memory of claim 1, where the at least three different categories comprise five categories comprising a first logic value~~low~~ resistive state category and a second logic value~~high~~ resistive state category.

4. (Original) The magnetic memory of claim 1, where the at least three different categories comprise an out-of-range low category.

5. (Original) The magnetic memory of claim 1, where the at least three different categories comprise an out-of-range high category.

6. (Original) The magnetic memory of claim 1, where the read circuit is configured to provide a read operation comprising multiple sense operations to obtain the sense result.

7. (Currently Amended) A magnetic memory, comprising:

an array of memory cells configured to provide resistive states; and

a read circuit configured to sense a resistance through a memory cell in the array of memory cells to obtain a sense result and categorize the sense result into one of at least three different categories comprising a middle category situated between the resistive states~~The magnetic memory of claim 1~~, where the read circuit is configured to provide a read operation comprising multiple sense operations to obtain the sense result, where the sense result from a shorted memory cell is categorized into the middle category.

8. (Currently Amended) A magnetic memory, comprising:

an array of memory cells configured to provide resistive states; and

a read circuit configured to sense a resistance through a memory cell in the array of memory cells to obtain a sense result and categorize the sense result into one of at least three different categories comprising a middle category situated between the resistive states~~The magnetic memory of claim 1~~, where the read circuit is configured to provide a read operation comprising multiple sense operations to obtain the sense result, where the sense result from an open memory cell is categorized into the middle category.

9. (Original) The magnetic memory of claim 1, where the read circuit is configured to provide a flag that indicates the sense result category.

10. (Original) The magnetic memory of claim 1, where the read circuit is configured to provide a logic level output.

11. (Original) The magnetic memory of claim 1, where the read circuit is configured to categorize the sense result after a first sense operation.

12. (Original) The magnetic memory of claim 1, where the sense result is a count and the count is compared to threshold values to categorize the count.

13. (Original) The magnetic memory of claim 1, where the read circuit comprises:

a direct injection charge amplifier configured to provide a sense current through the memory cell;

a capacitor configured to provide the sense current to the direct injection charge amplifier; and

a sense amplifier configured to provide a count based on the time it takes for the capacitor to decay to a reference voltage.

14. (Currently Amended) A magnetic memory, comprising:

an array of memory cells;

means for reading the memory cells in the array of memory cells to obtain read operation results; and

means for categorizing the read operation results into categories comprising a category between a first logic value~~low~~ resistive state category and a second logic value~~high~~ resistive state category.

15. (Original) The magnetic memory of claim 14, where the means for reading the memory cells comprises a read circuit configured to provide multiple sense operations in a read operation to obtain a net count as one of the read operation results.

16. (Original) The magnetic memory of claim 14, where the means for categorizing is configured to receive a net count from the means for reading the memory cells and categorize the net count into one of the categories.

17. (Currently Amended) A magnetic memory, comprising:

a memory cell; and

a read circuit configured to sense a resistance through the memory cell to obtain a sense result and provide immediate calibration if the sense result indicates a shorted memory cell and if the sense result indicates an open memory cell, and delayed calibration if the sense result indicates the resistance is greater than a shorted memory cell and less than a first logic value~~low~~ resistive state of the memory cell and if the sense result indicates the resistance is

less than an open memory cell and greater than a second logic value ~~high~~ resistive state of the memory cell.

18. (Original) The magnetic memory of claim 17, where the read circuit is configured to categorize the sense result into categories comprising a short category, an open category, a low delayed calibration category and a high delayed calibration category.

19. (Currently Amended) The magnetic memory of claim 17, where the read circuit is configured to provide a first sense result from a first sense operation as the sense result and categorize the sense result into categories comprising a no calibration category that comprises first logic value~~low~~ resistive state values and second logic value~~high~~ resistive state values and provide a net result from a multiple sense read operation and categorize the net result into one of a plurality of categories based on the net result.

20. (Currently Amended) The magnetic memory of claim 19, where the plurality of categories comprises a middle category between the first logic value~~low~~ resistive state values and the second logic value~~high~~ resistive state values of the memory cell.

21. (Currently Amended) The magnetic memory of claim 19, where the plurality of categories comprises a dubious category, a first logic value~~low~~ resistive state category and a second logic value~~high~~ resistive state category, and the dubious category is situated between the first logic value~~low~~ resistive state category and the second logic value~~high~~ resistive state category.

22. (Currently Amended) A method of reading a magnetic memory, comprising:

sensing resistance through a memory cell of the magnetic memory to obtain a net sensed result value; and

categorizing the net sensed result value into a plurality of different resistive regions comprising a first logic value~~low~~ resistive state region, a second logic value~~high~~ resistive state region and a middle region situated between the first logic value~~low~~ resistive state region and the second logic value~~high~~ resistive state region.

23. (Original) The method of claim 22, where sensing resistance through the memory cell comprises a multiple sense read operation comprising three sense operations.

24. (Original) The method of claim 22, where the net sensed result value is a count that corresponds to resistances sensed through the memory cell.

25. (Original) The method of claim 22, where categorizing the net sensed result value comprises comparing the net sensed result value to thresholds and providing a flag to indicate the net sensed result value region.

26. (Original) A method of reading a magnetic memory, comprising:

sensing a memory cell to obtain a first sense result;

categorizing the first sense result into regions comprising immediate calibration and delayed calibration regions; and

responding based on the category of the first sense result.

27. (Original) The method of claim 26, where responding comprises providing an immediate calibration response if the first sense result is an open and if the first sense result is a short.

28. (Currently Amended) The method of claim 27, where responding comprises providing a delayed calibration response if the first sense result is between a short and a first logic value~~low~~ resistive state value and if the first sense result is between an open and a second logic value~~high~~ resistive state value.

29. (Original) The method of claim 28, comprising:

sensing the memory cell in a multiple sense read operation to obtain a final result;

categorizing the final result.

30. (Currently Amended) The method of claim 29, where categorizing the final result comprises situating the final result into one of a plurality of regions comprising first logic value~~low~~ resistive state and second logic value~~high~~ resistive state regions.

31. (New) A magnetic memory, comprising:

an array of memory cells configured to provide logic 0 and logic 1 resistive states; and

a read circuit configured to sense a resistance through a memory cell in the array of memory cells to obtain a sense result and categorize the sense result into one of at least three different categories comprising a middle category situated between the logic 0 and logic 1 resistive states.

32. (New) The magnetic memory of claim 31, where the at least three different categories comprise five categories including a logic 0 resistive state category, a logic 1 resistive state category, an out-of-range low category, and an out-of-range high category.